

# Compal Confidential

**ZAWBA/ZAWBB**  
**DIS M/B Schematics Document**  
**AMD Beema SOC with DDR3L**

**AMD Jet LE**

**2014-03-03**

**LA-B291P**

**REV : 1.0**

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VRAM 1G/2G  
256M16 x 4 (2G)  
128M16 x 4 (1G)

DDR3L

AMD Jet LE

VRAM 1GB/2GB  
DDR3L x4

PCIe x 4 Gen2

AMD Beema

Memory BUS(DDR3L)

Single Channel

204pin DDR3L SO-DIMM X2

BANK 0, 1, 2

1.35V DDR3L 1600MHz

eDP Conn.

HDMI Conn.

CRT Conn.

GPP0

GPP2

GPP1

Card Reader  
Realtek

RTS5229

NGFF  
(WLAN/BT)

LAN 10/100/1G  
Realtek

8111G/8106E

Transformer  
RJ45

SPI ROM (8MB)

Nuvoton  
NPCE288NB0DX

Int.KBD

Touch Pad

Thermal Sensor

GFX

DP0

DP1

DAC

GPP

SPI

LPC

AMD FT3b APU

BGA 769-balls

USB

USB

HDA

SATA

USB2.0

MB  
3.0 Conn. LP1

USB3.0

HD Audio

Gen3 Port 0

Port 1

HDD  
Conn.

ODD  
Conn.

Audio  
Realtek

ALC233VB

Int. MIC

Int. Speaker Conn.

Audio Combo Jacks

In IO/B

14" Sub-borad

15" Sub-borad

IO/B  
USB2.0 x 1  
Combo Jack  
Novo button

LED/B

14" Power/B

IO/B  
USB2.0 x 1  
Combo Jack  
Novo button

LED/B

Battery/B

15" Power/B

ODD/B

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## Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.35V	1.35V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.35VGS	1.35V switched power rail for VGA	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF

## BOARD ID Table

Board ID	PCB Revision
0	MP
1	PVT
2	DVT
3	EVT
4	
5	
6	
7	

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R1562	100K +/- 5%			
Board ID	R1564	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

## USB OC MAPPING

OC#	USB Port
0	USB20 port0
1	USB20 port1,2,8,9
2	
3	

## BOM Structure Table

BOM Structure	BTO Item
45@	for HDMI Logo
14@	for 14" component
15@	for 15" component
B5@	15W 2.4GHz BGA APU
B4@	15W 1.8GHz BGA APU
B3@	15W 1.5GHz BGA APU
B2@	10W 1.5GHz BGA APU
B1@	10W 1.35GHz BGA APU
UMA@	UMA part
PX@	Common VGA circuit
JET@	Jet LE GPU
TOPAZ@	Topaz XT GPU
CMOS@	CMOS Camera part
HDMI@	HDMI part
8106ELDO@	Realtek RTL8106E with LDO mode
8106ESW@	Realtek RTL8106E with SWR mode
8111GLDO@	Realtek RTL8111G with LDO mode
8111GSW@	Realtek RTL8111G with SWR mode
TS@	Touch Screen
ZODD@	Zero Power ODD part
NOZODD@	Non-Zero Power ODD part
CHG@	USB Charger function
NOCHG@	Non-USB Charger function
FHD@	Full HD Panel
DR@	VRAM Dual Rank
SR@	VRAM Single Rank
USB2@	USB 2.0
USB3@	USB 3.0
233VB@	Realtek ALC233-VB Audio IC
ME@	ME part
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component
GIGAEMIP@	EMI Un pop for LAN GIGA function
@	Unpop

## SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	288N +3VALW	X	V +3VALW	X	X	X	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	288N +3VS	V +3VS	X	X	X	X	V +3VS	X	V +3VS	X

## APU PCIE PORT LIST

Port	Device
0	Card Reader
1	LAN
2	WLAN
3	

## USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
		0	Touch Screen
		1	RIGHT USB
		2	
		3	Camera
		4	
		5	WLAN/BT Combo
		6	
		7	Finger Print
	XHCI	0	LEFT USB3.0
		1	LEFT USB3.0

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Thermal Sensor	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

## APU SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H
DDR DIMM2	1010 001Xb	A2H

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## Jet LE VRAM STRAP

		X76@			X76@			
		Vendor UV5, UV6, UV7, UV8	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV21	R_pd RV24
1GBytes	ZZZ09 JH1G@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	0	0	0	0	NC	4.75K
1GBytes	ZZZ10 JM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	0	0	1	8.45K	2K
1GBytes	ZZZ11 JS1G@	Samsung 2048Mbits SA000068U40 128Mx16 K4W2G1646Q-BC1A	2	0	1	0	4.53K	2K
2GBytes	ZZZ12 JH2G@	Hynix 4096Mbits SA00006E800 256Mx16 H5TC4G63AFR-11C	3	0	1	1	6.98K	4.99K
2GBytes	ZZZ13 JS2G@	Samsung 4096Mbits SA000076P00 256Mx16 K4W4G1646D-BC1A	4	1	0	0	4.53K	4.99K
2GBytes	ZZZ14 JM2G@	Micron 4096Mbits SA000077K00 256Mx16 MT41J256M16HA-093G:E	5	1	0	1	3.24K	5.62K
2GBytes	ZZZ08 JM2G2@	Micron 4096Mbits SA000065D00 256Mx16 MT41K256M16HA-107G:E	6	1	1	0	3.4K	10K
1GBytes	ZZZ16 JM1G2@	Micron 2048Mbits SA00005XB00 128Mx16 MT41K128M16JT-107G:K	7	1	1	1	4.75K	NC



R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

**Note:** 0402 1% resistors are required.

## Power-Up/Down Sequence

"Jet" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- It is recommended that the 3.3-V rail ramp up first.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpress™ idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as  $\leq 50\text{mV/us}$ ).
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

VDDR3(+3VGS)

PCIE\_VDDC(+0.95VGS)

VDDR1(+1.35VGS)

VDDC/VDDCI(+VGA\_CORE)

VDD\_CT(+1.8VGS)

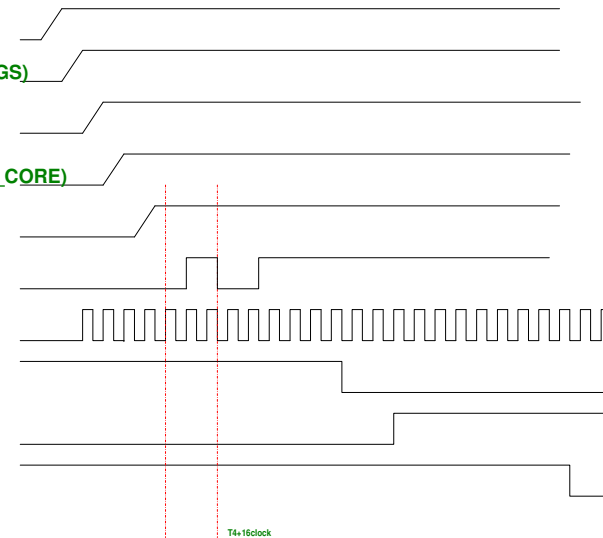
PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset

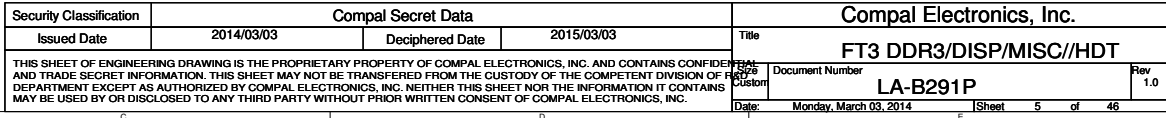


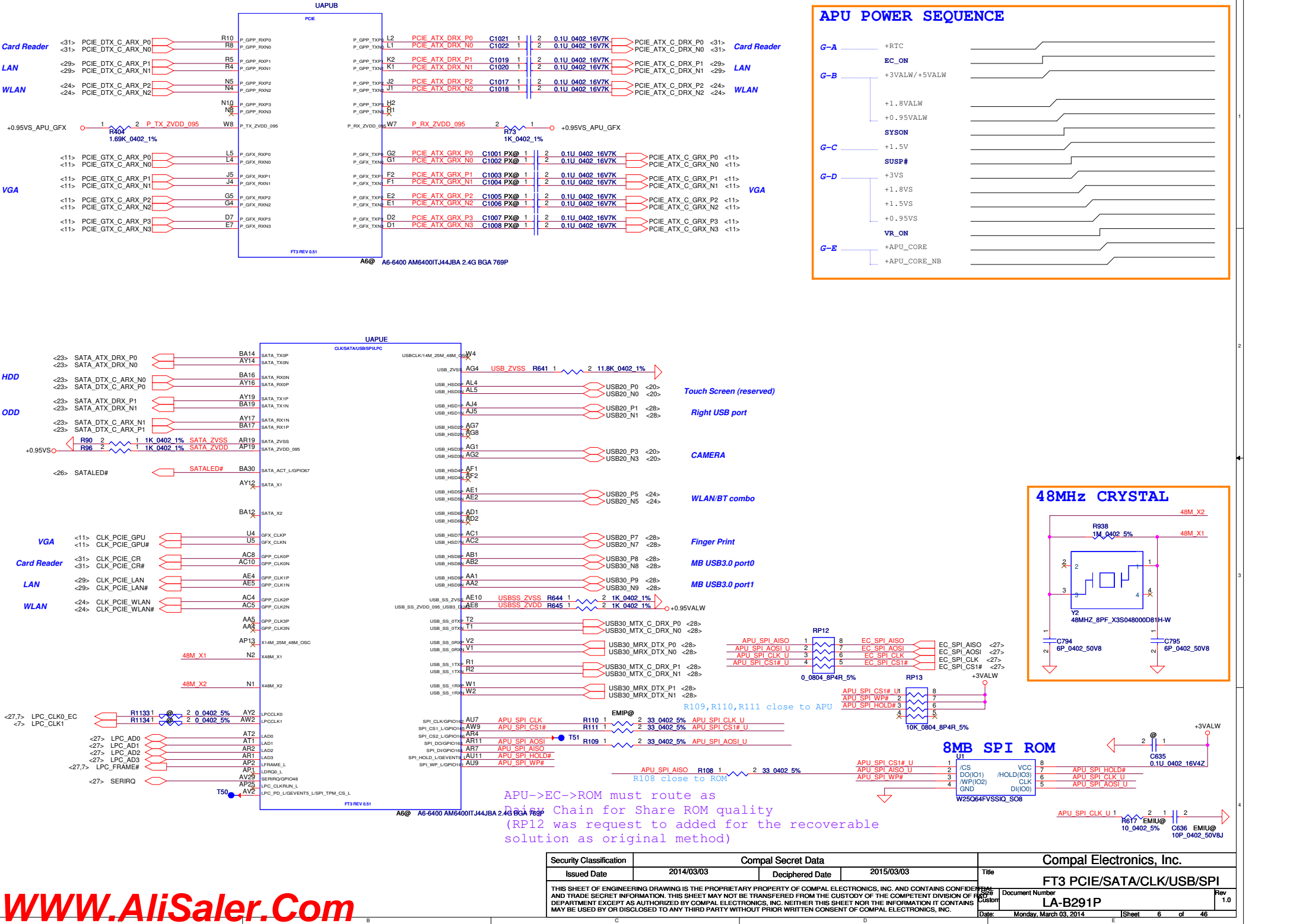
T4+16clock

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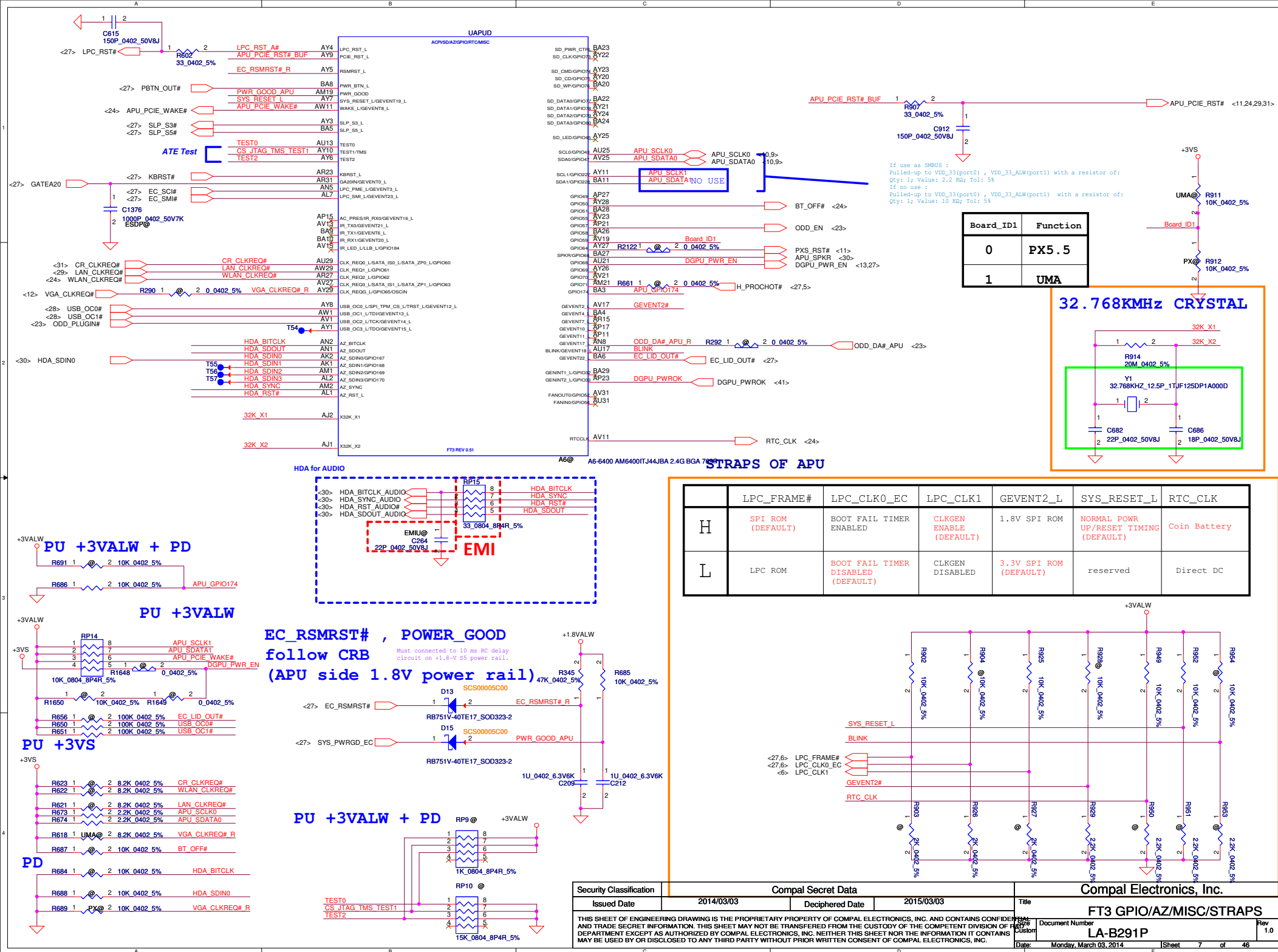
VGA Notes List

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W=20mils

R93 1 2 10K\_0402\_5%

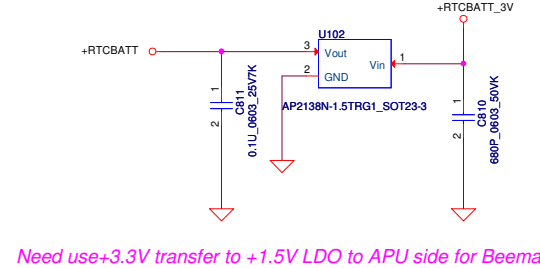
C1365 1 2 0.22U\_0402\_10V6K

CLRP1 @ Need OPEN  
SHORT PADS

for Clear CMOS

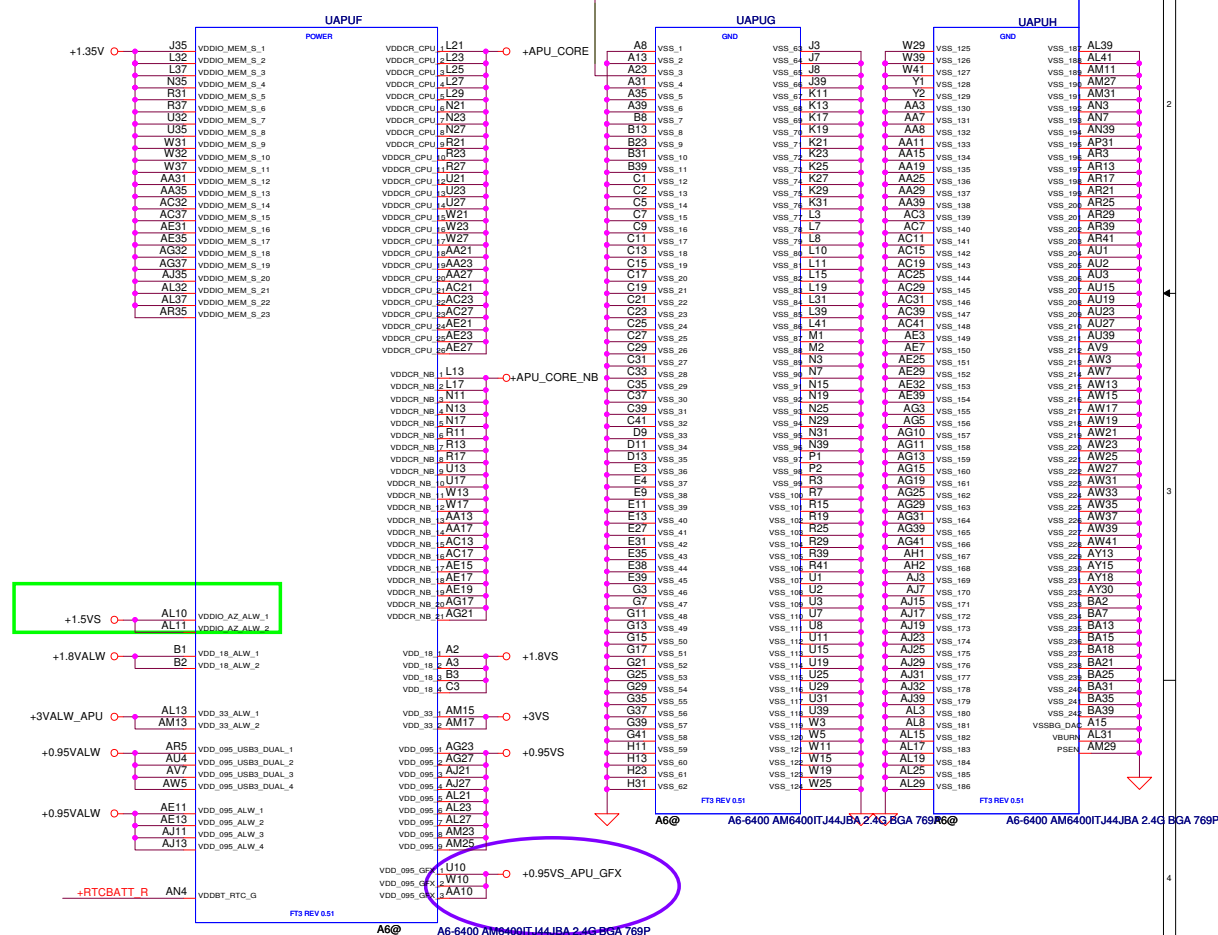
+RTCBATT\_R

+RTCBATT 需過LDO轉1.5V, 20130930 added



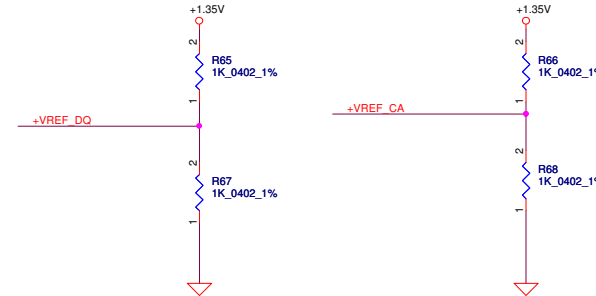
Timing diagram for the 74VHC04 hex inverters. The diagram shows the input and output signals for six inverters (C1259 to C1264) over a period of 10 ns. The input signals are labeled C1259, C1258, C1257, C1256, C1255, and C1254. The output signals are labeled C1264, C1263, C1262, C1261, C1260, and C1259. The input signals are shown as a series of pulses, and the output signals are shown as inverted pulses. The timing diagram includes a 10 ns scale bar and a ground symbol.

The schematic diagram illustrates the input stage of a 741 op-amp. It features a differential pair of NPN transistors, C1254 and C1255, with their emitters connected to a common emitter resistor, C1256, which is grounded. The bases of these transistors are biased by a voltage divider consisting of C1232 and C1233, connected to a 5.0V supply. The collector of C1254 is connected to a load resistor, C1257, and a feedback network consisting of C1258 and C1259, which leads to the output. The collector of C1255 is connected to a similar load resistor, C1257, and a feedback network consisting of C1258 and C1259, which leads to the output. The output is taken from the collector of C1254.



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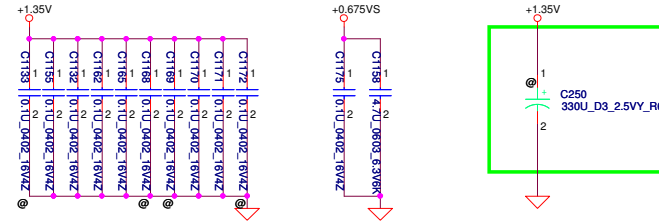
**DIMM\_A H:4mm**  
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# JDIMM1 Standard Type Near User

DDRAB\_SDQ[0..63] DDRAB\_SDQ[0..63] <5.9>  
DDRAB\_SDM[0..7] DDRAB\_SDM[0..7] <5.9>  
DDRAB\_SMA[0..15] DDRAB\_SMA[0..15] <5.9>

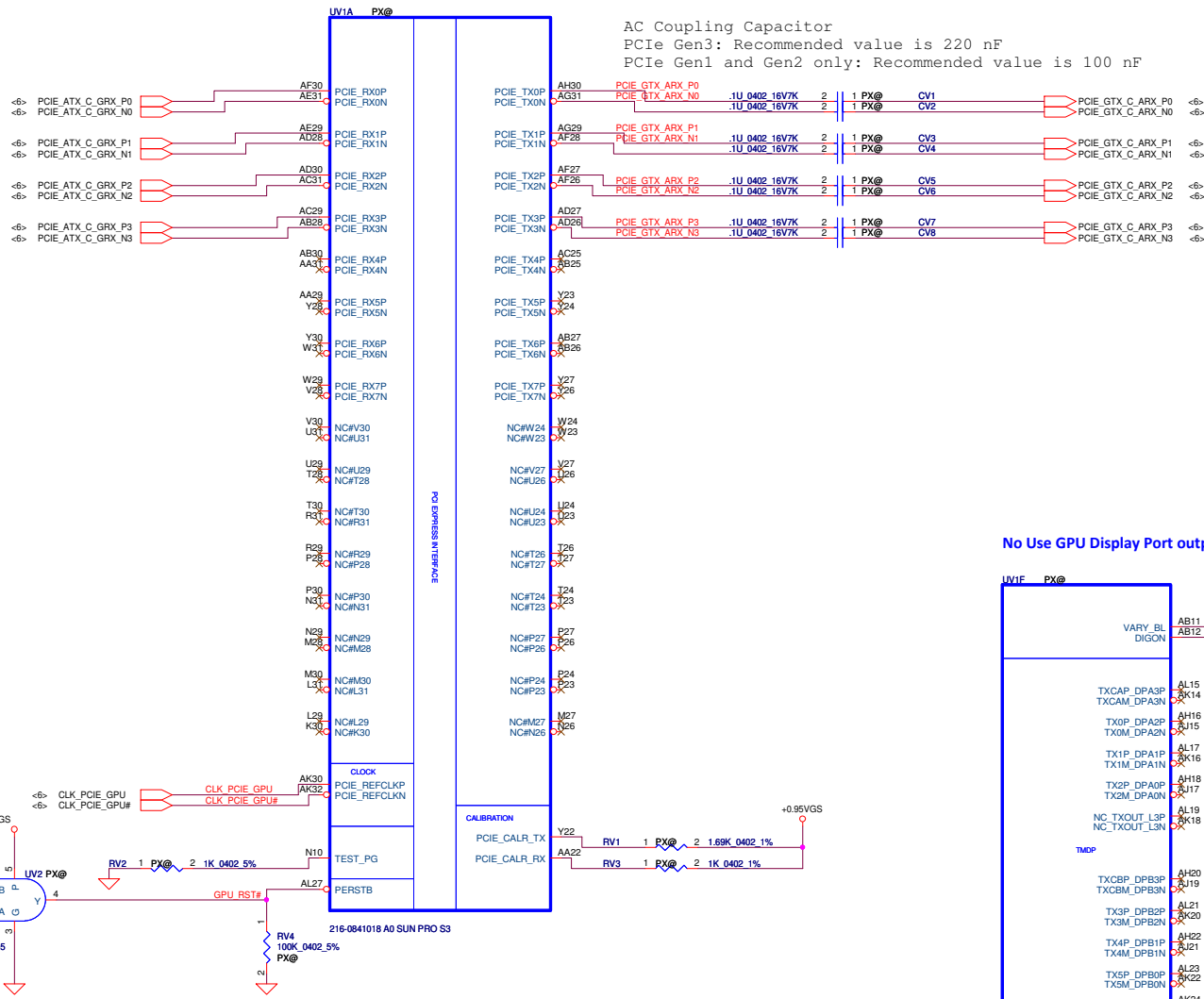
+1.35V/+0.675VS OF DIMM2



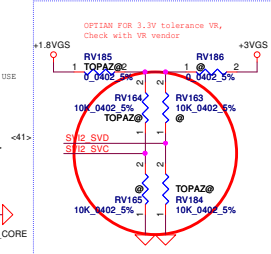
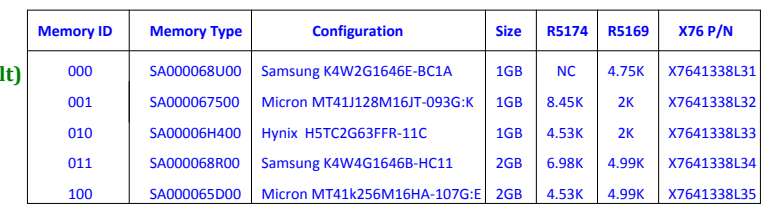
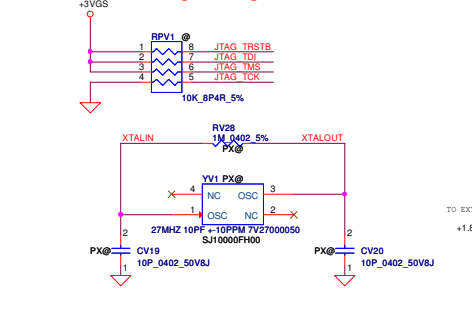
DIMM\_B H:4mm

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**+1.35VS to +1.35VGS**



**ANSWER:** **C**

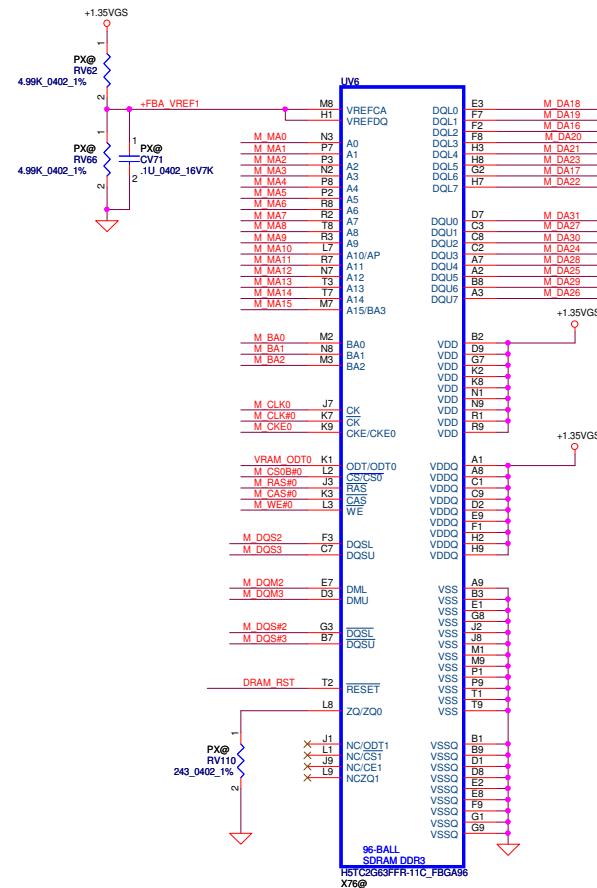


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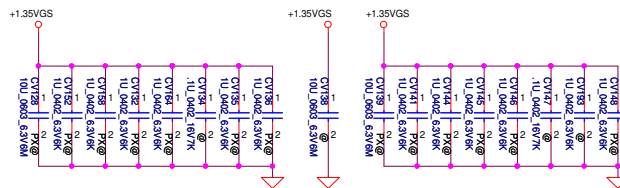
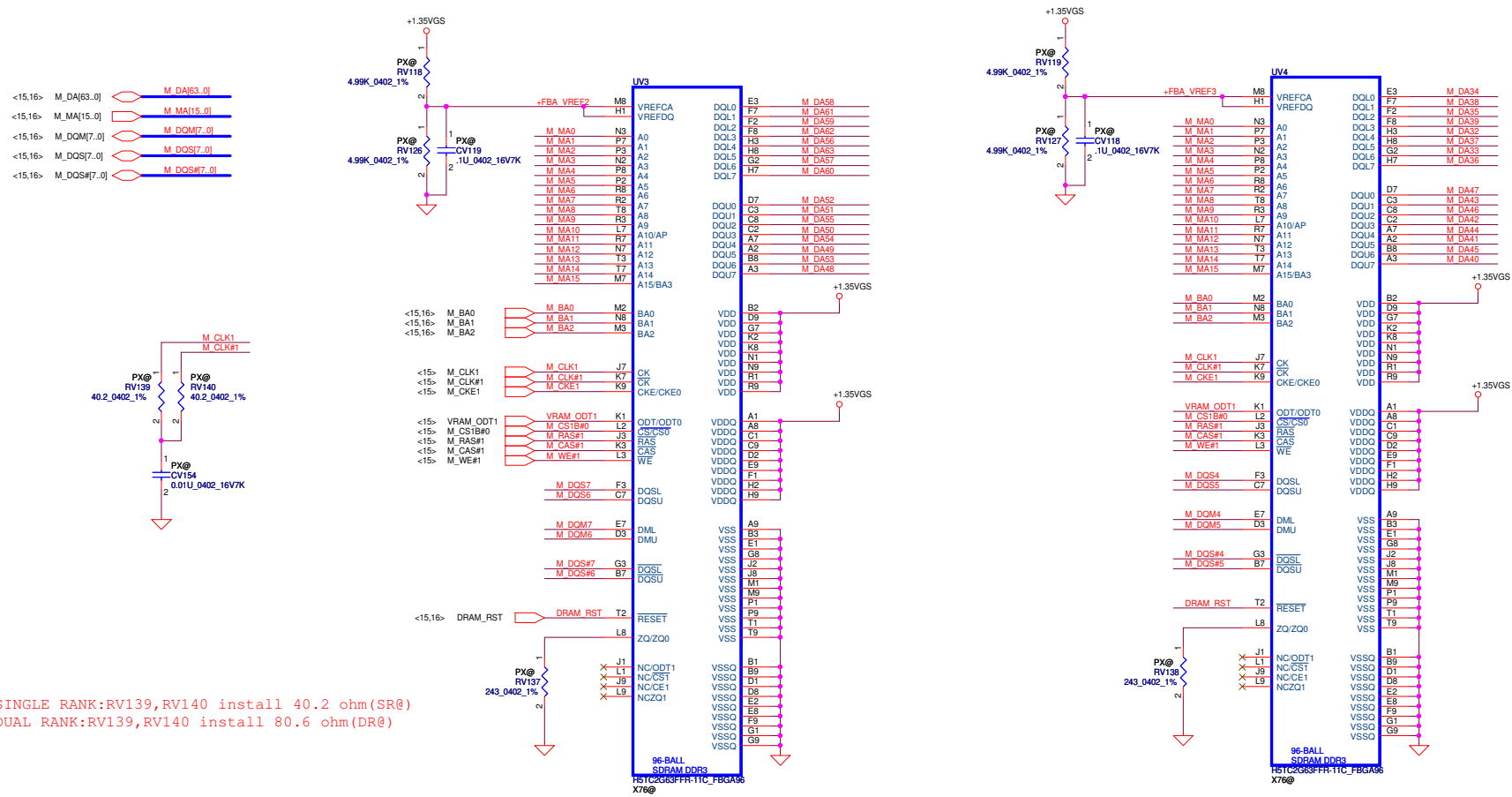


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## DDR3L Memory Channel Rank 0:A1



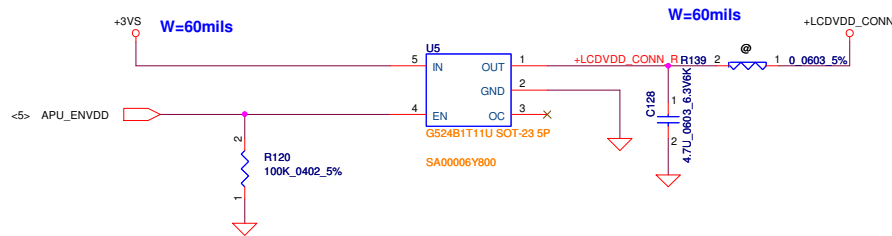
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Size A		Document Number LA-B291P																				Rev 1.0		
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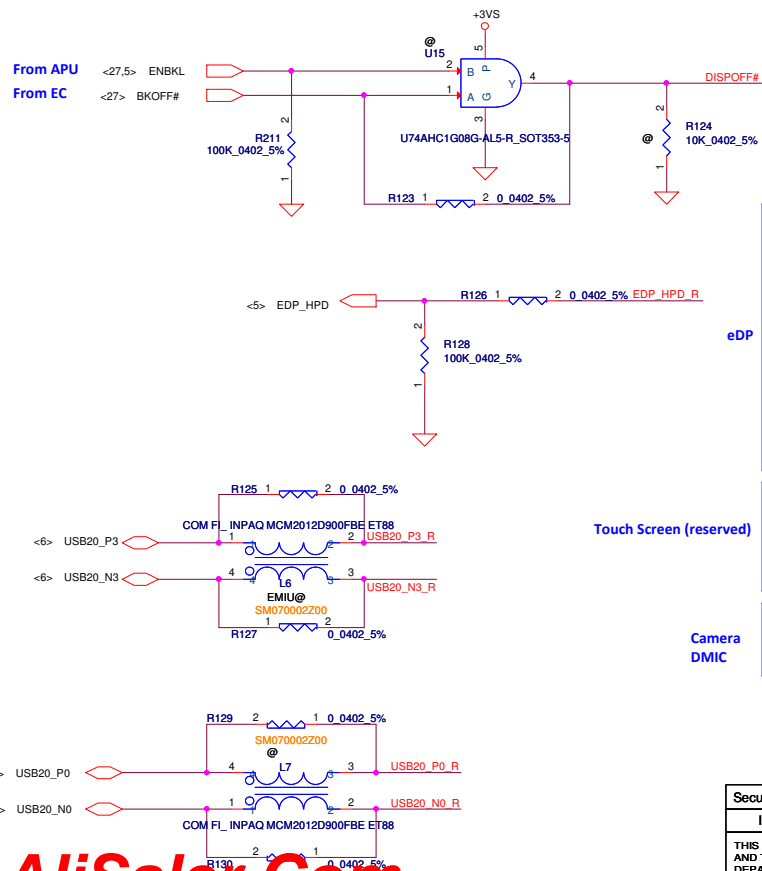
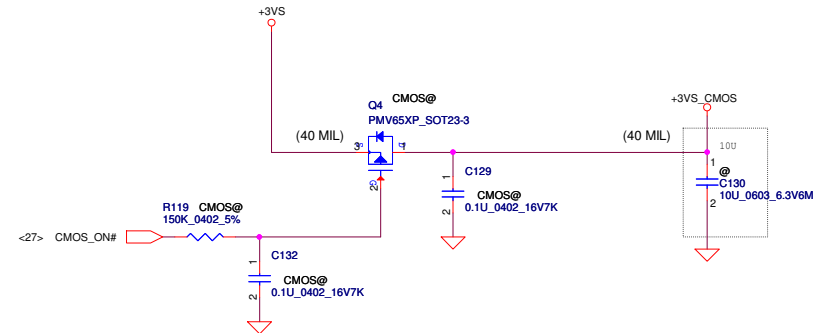
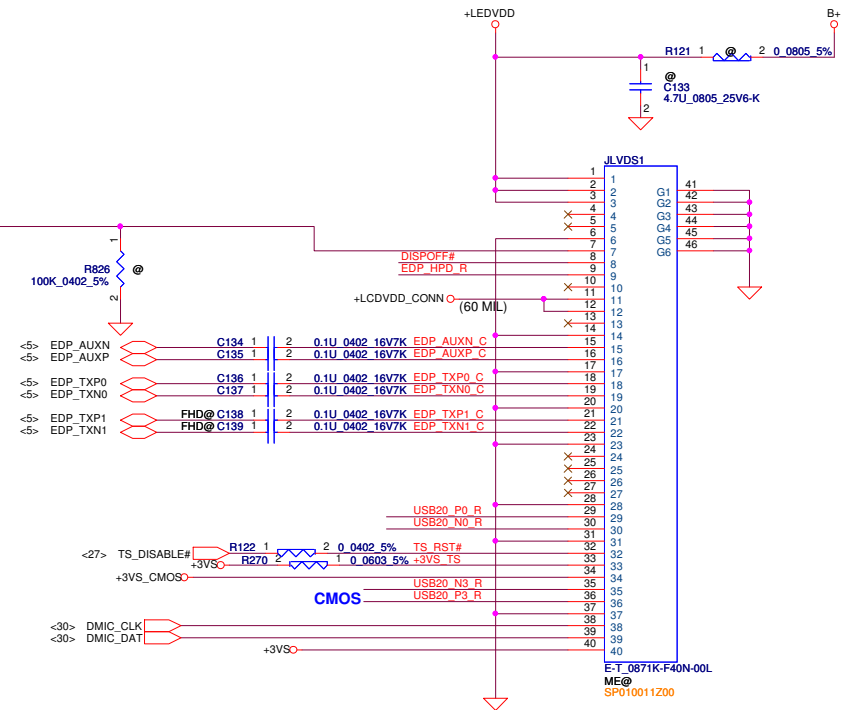
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## LCD POWER CIRCUIT

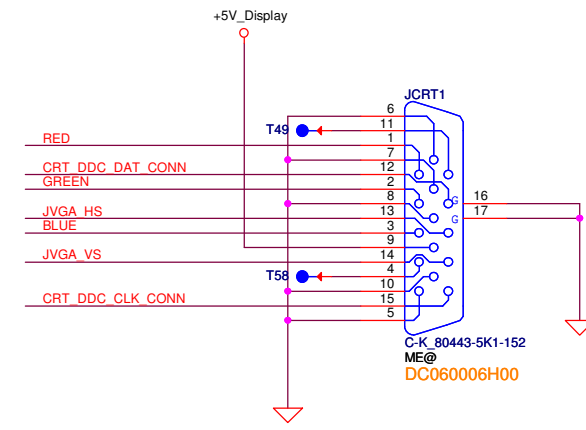
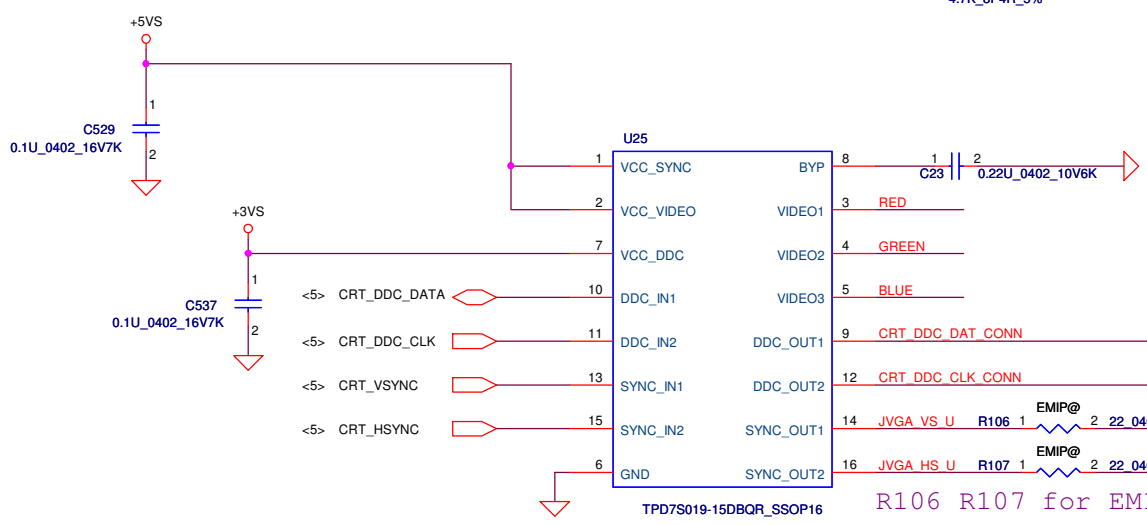
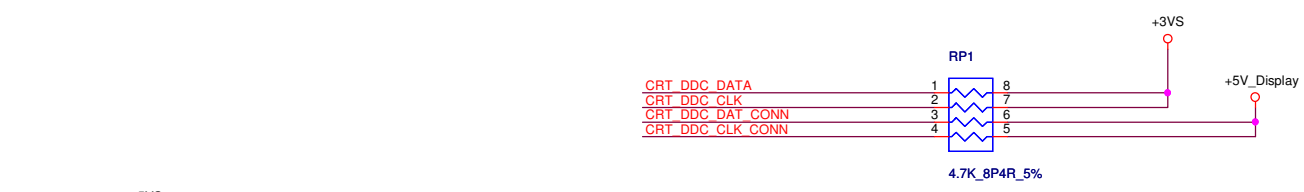
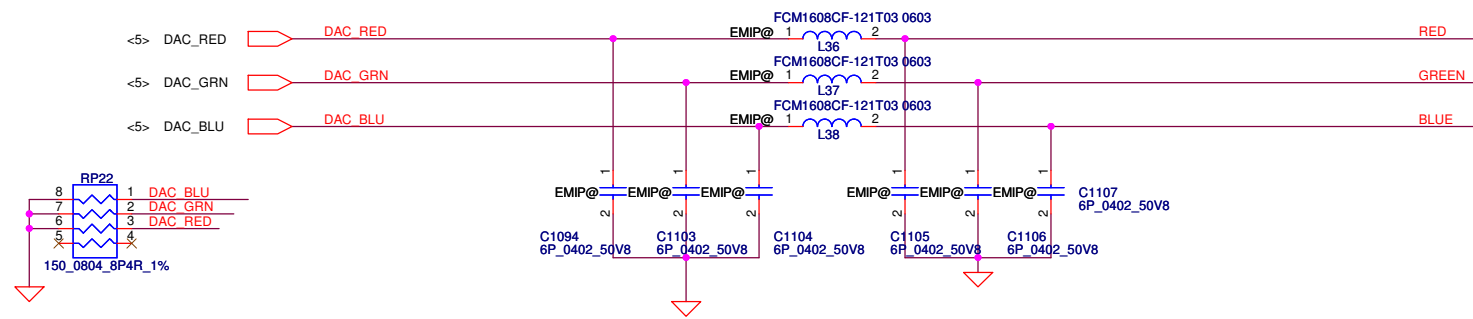


## CMOS Camera

**VGA LCD/PANEL BD. Conn.**

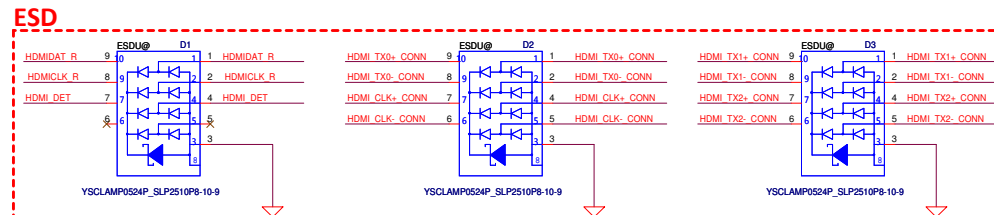
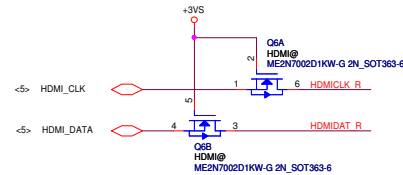
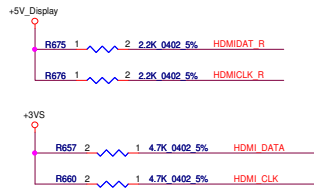
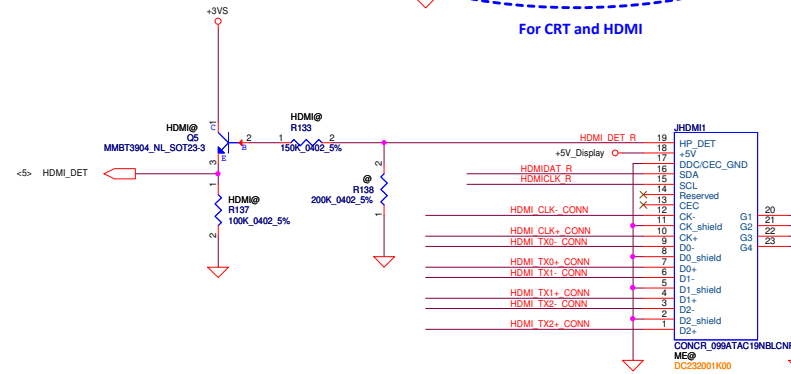
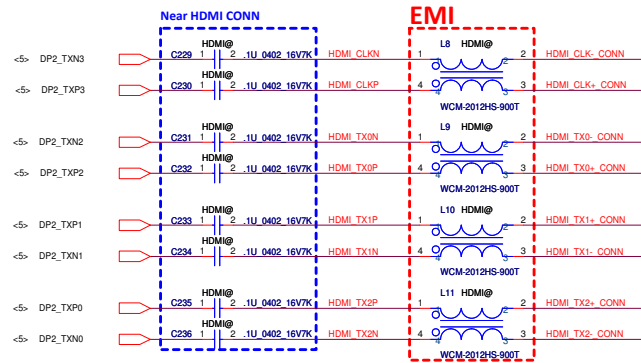
Security Classification		Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	EDP CONN / Camera		
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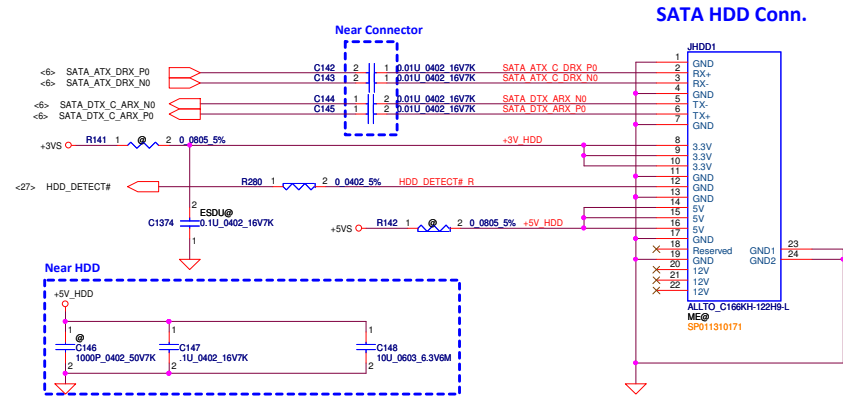
U25 have embeded ESD protection, and place it near CRT connector.

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				Date: Monday, March 03, 2014	Sheet 21 of 46

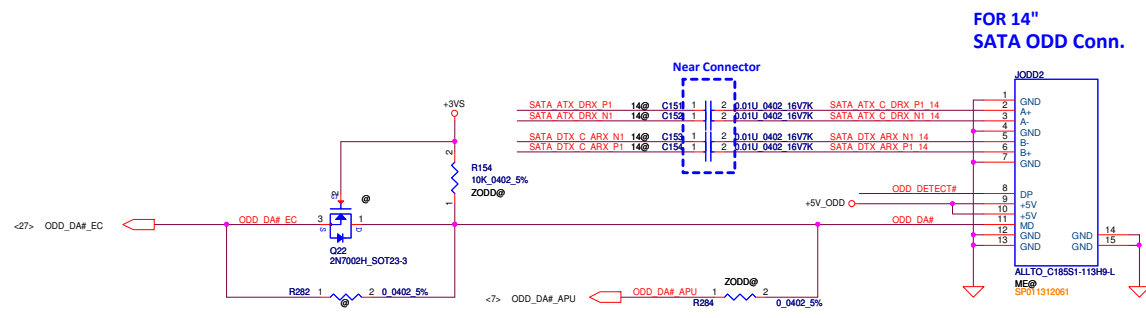
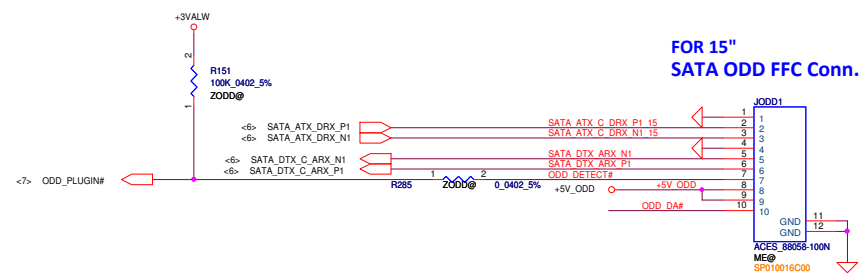
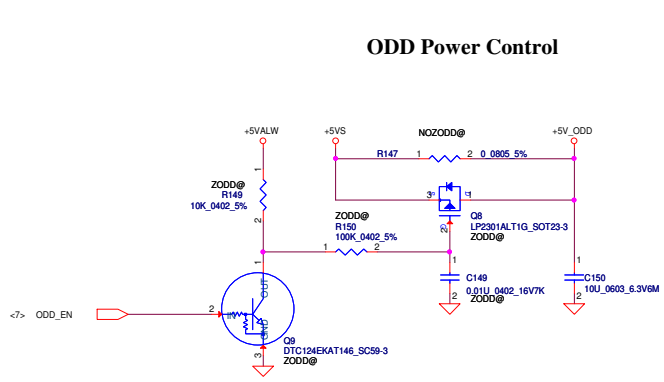


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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	HDMI CONN		
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				Date:	Monday, March 03, 2014		Sheet 22 of 46

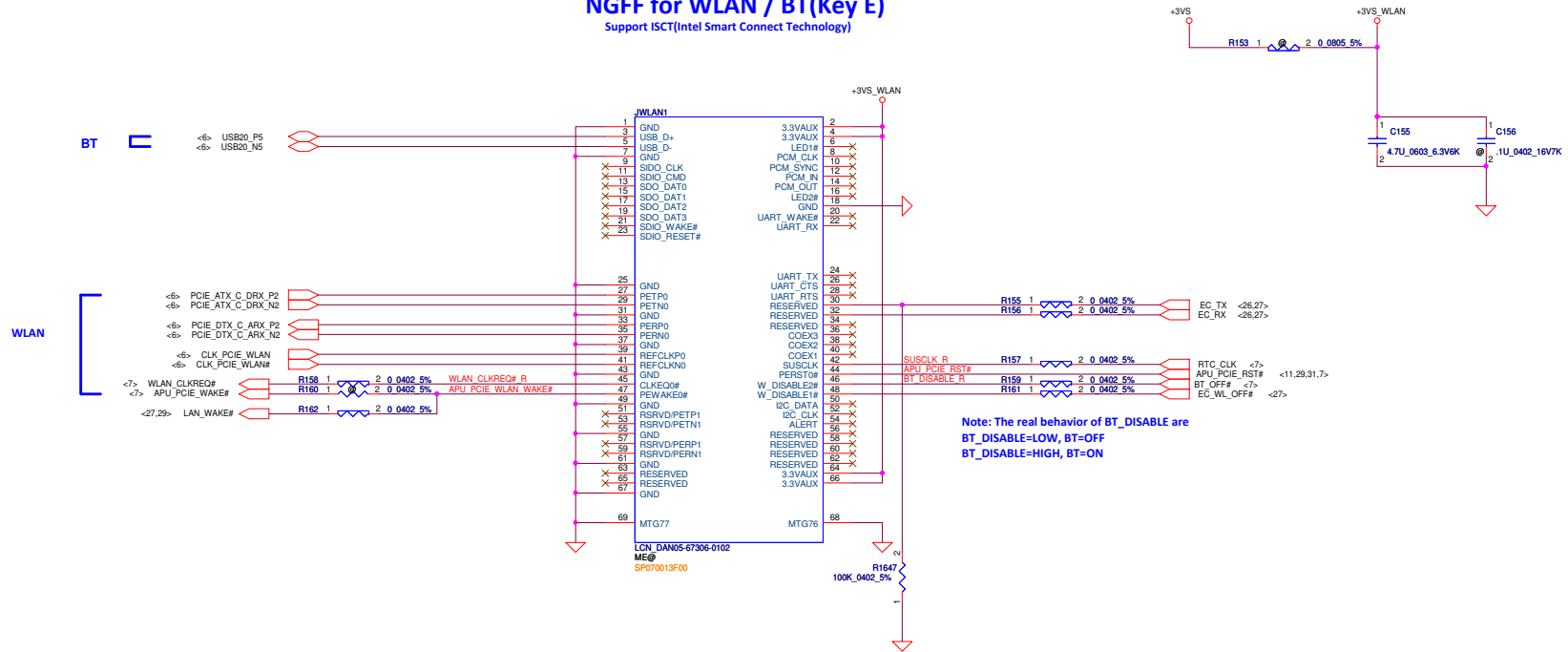
HDD



ODD

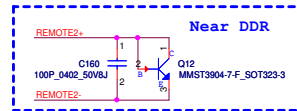


# NGFF for WLAN / BT(Key E) Support ISCT(Intel Smart Connect Technology)

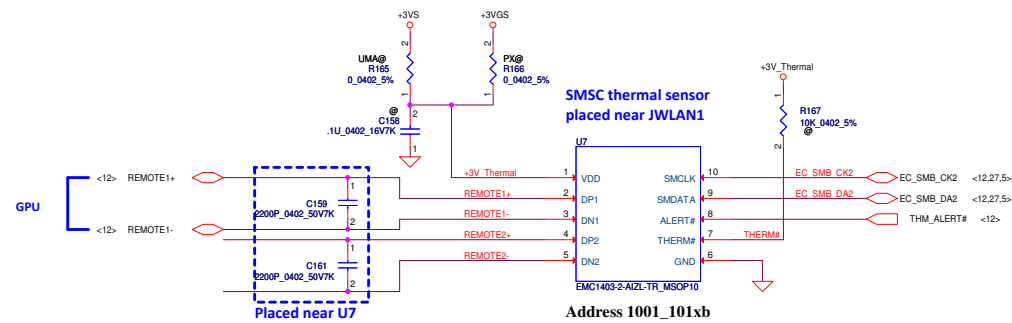


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Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	
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Size	C	Document Number	LA-B291P	Rev	1.0
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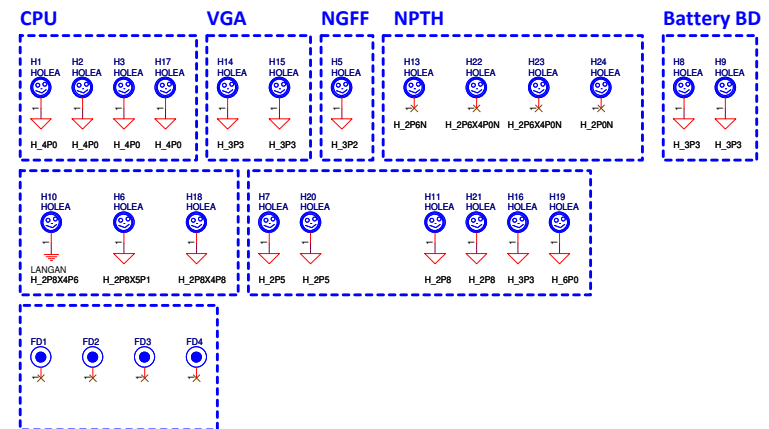
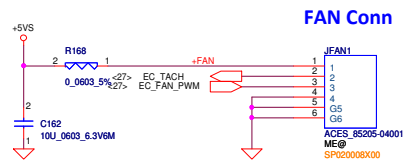
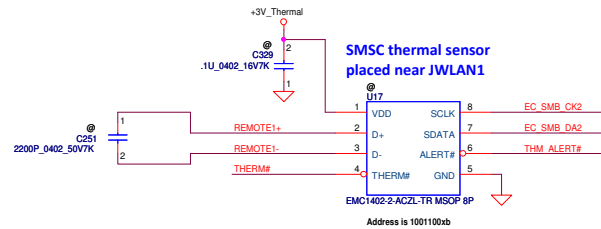
### 3 Channel



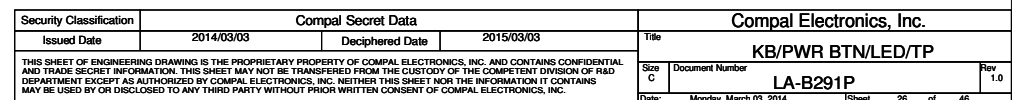
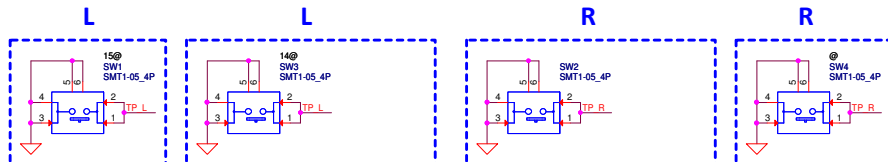
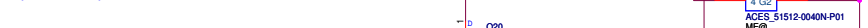
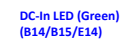
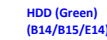
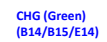
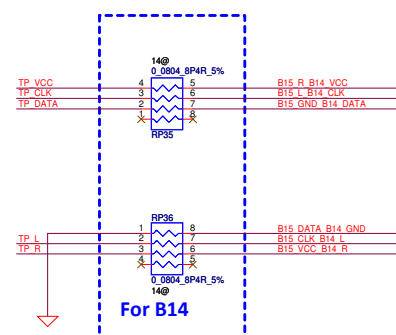
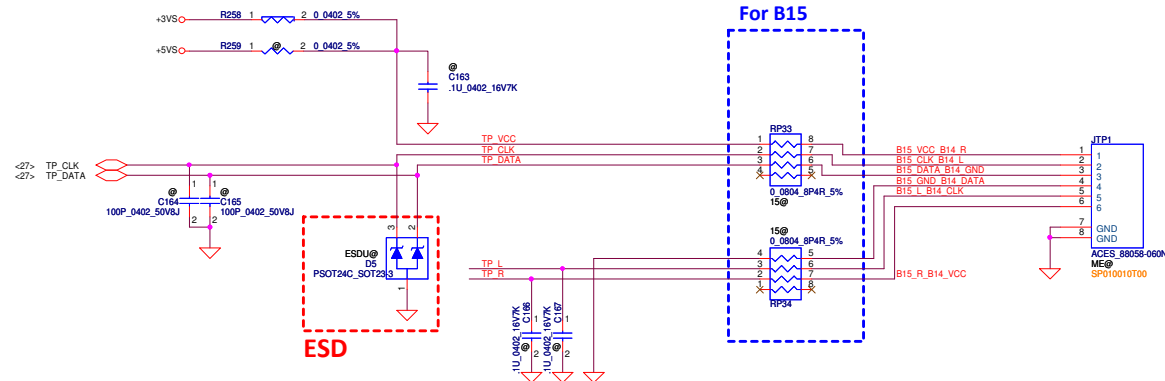
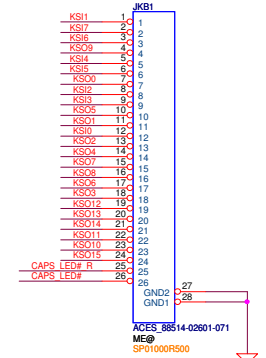
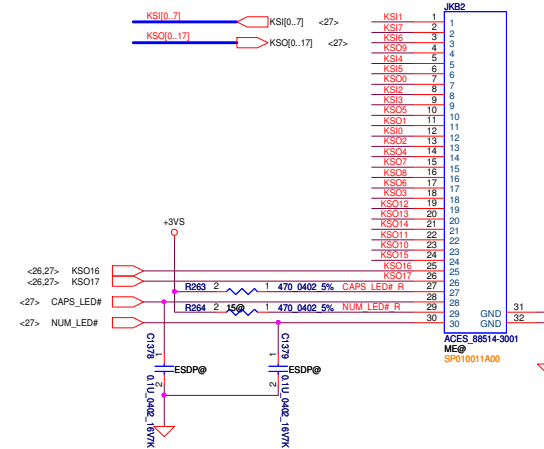
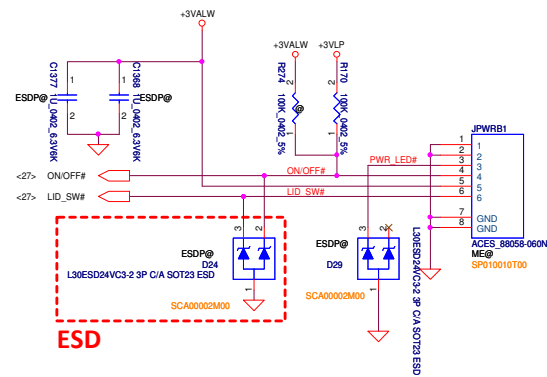
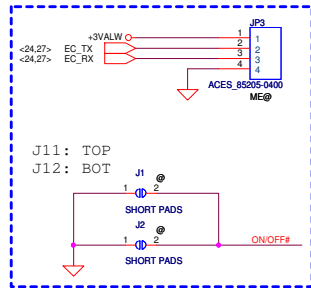
REMOTE1,2+/-:  
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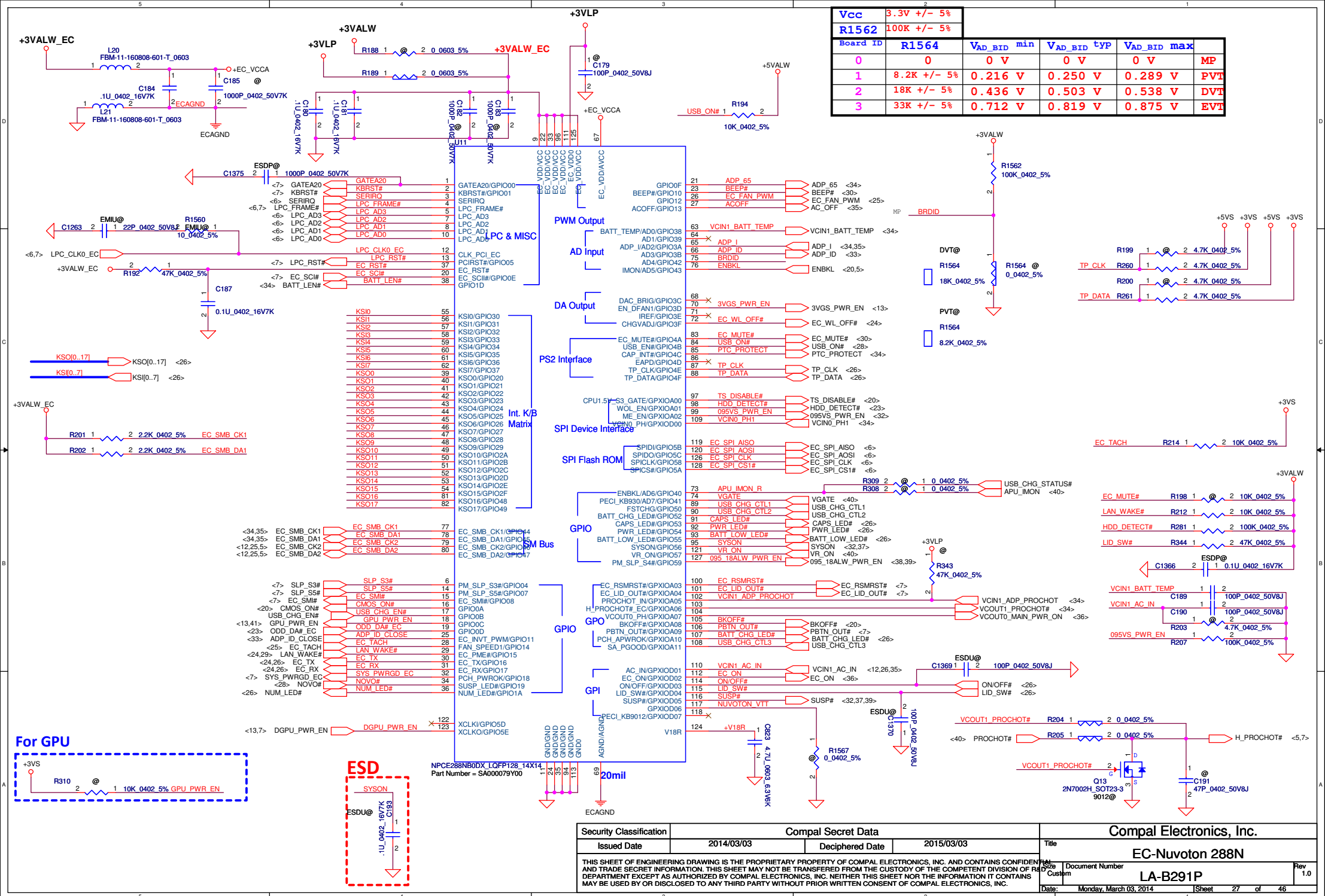


## 2 Channel

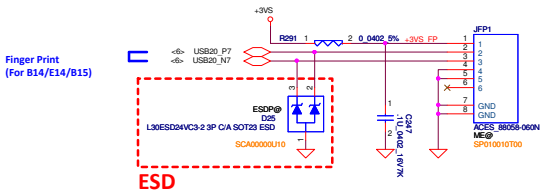


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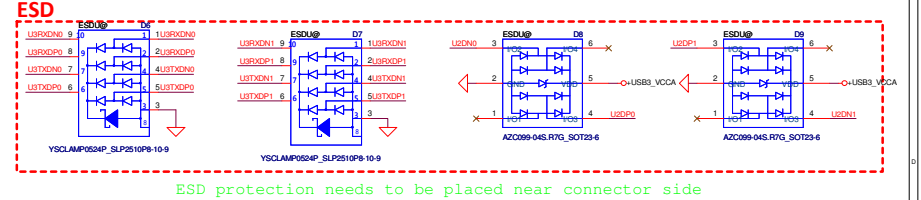
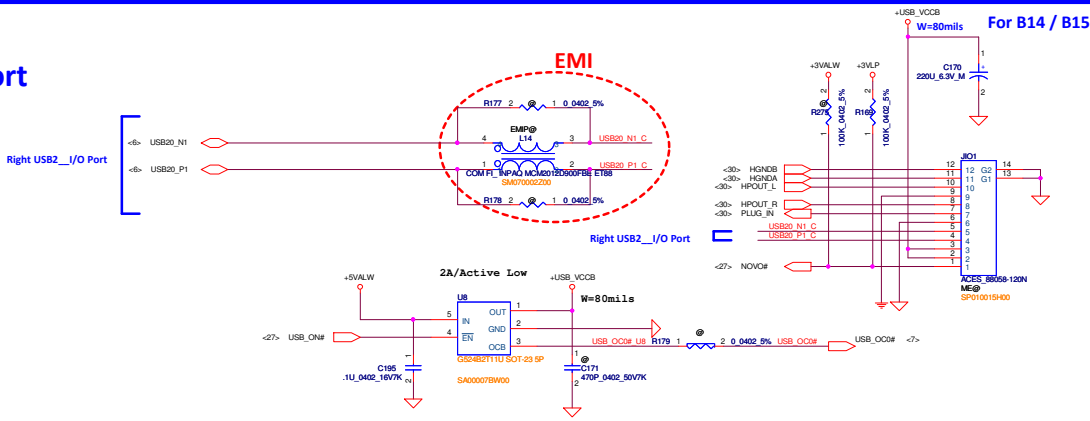




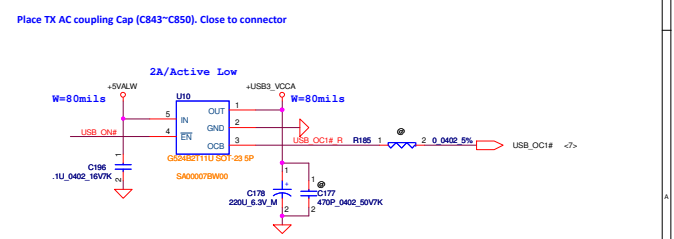
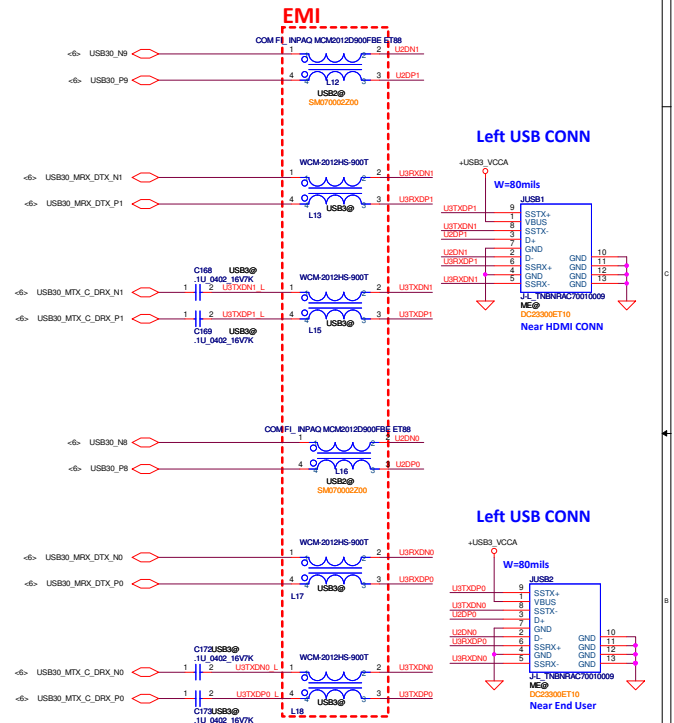
Finger Print



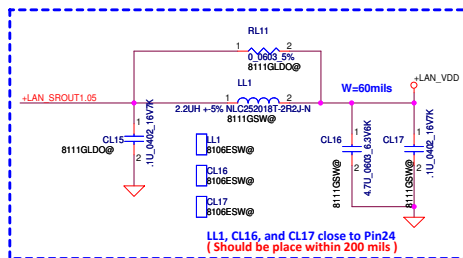
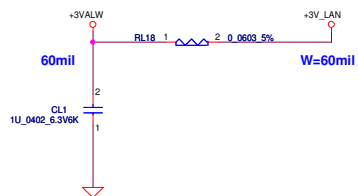
USB2.0\_Port



USB3.0\_Port



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				Date: Monday, March 03, 2014 Sheet 28 of 46

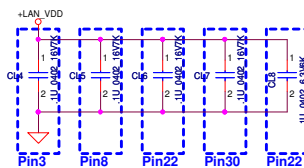
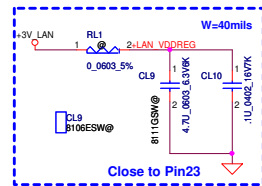
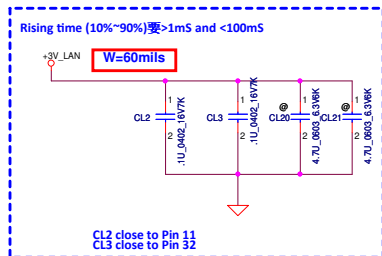


SA00005V700

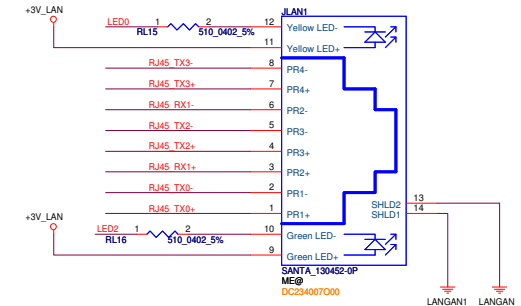
SA00005Y00

	1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
RTL8111G	LDO	X	X	X	O	O
RTL8111G	External	X	X	X	X	O
RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
RTL8106E	LDO	X	X	X	X	X

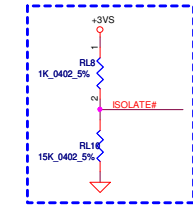
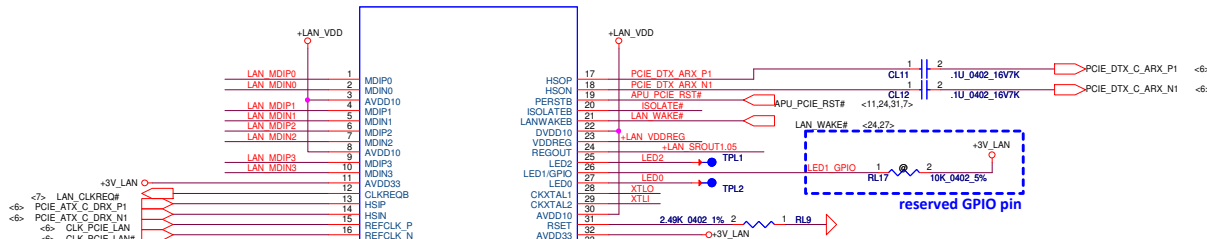
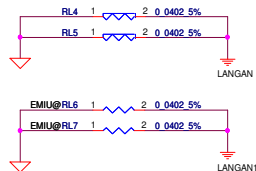
Please refer to the table above when using different 1.0V supply source.  
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.



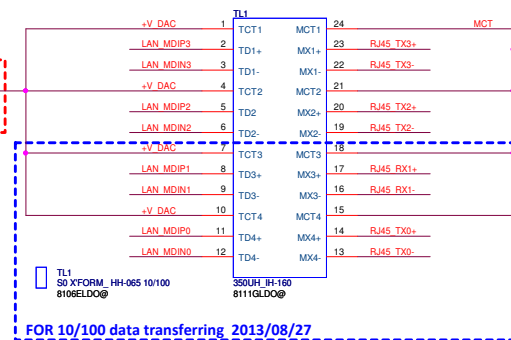
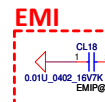
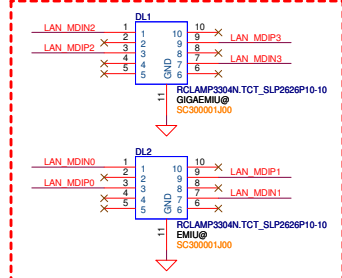
## RJ-45 CONN.



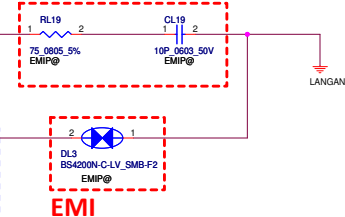
## EMI



## EMI

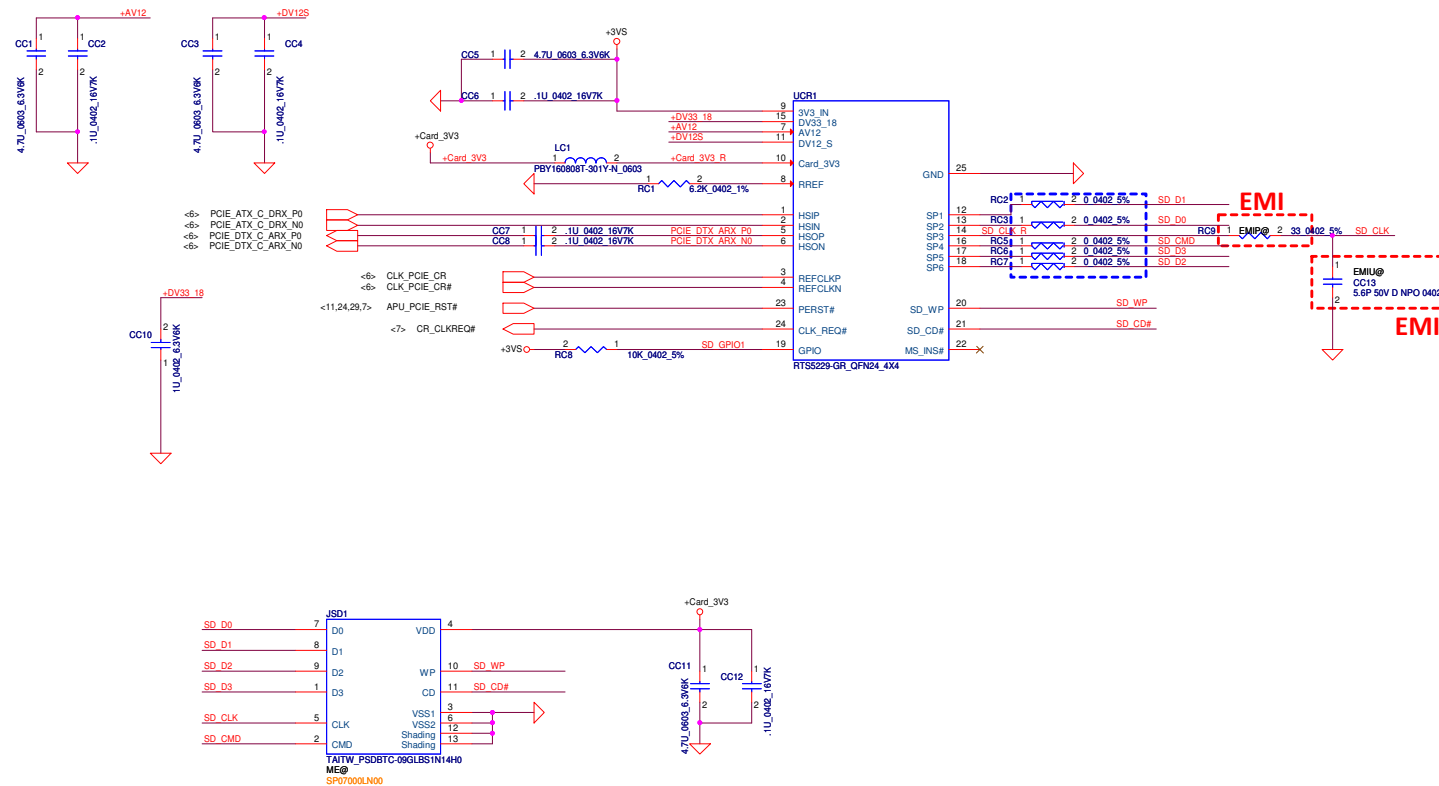


## EMI

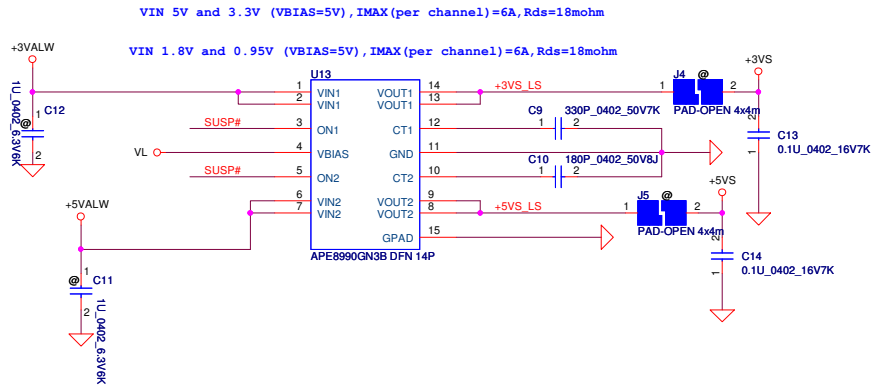


Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2014/03/03	Deciphered Date
2015/03/03		
Size	Document Number	Rev
C	LA-B291P	1.0
Date	Monday, March 03, 2014	Sheet 29 of 46

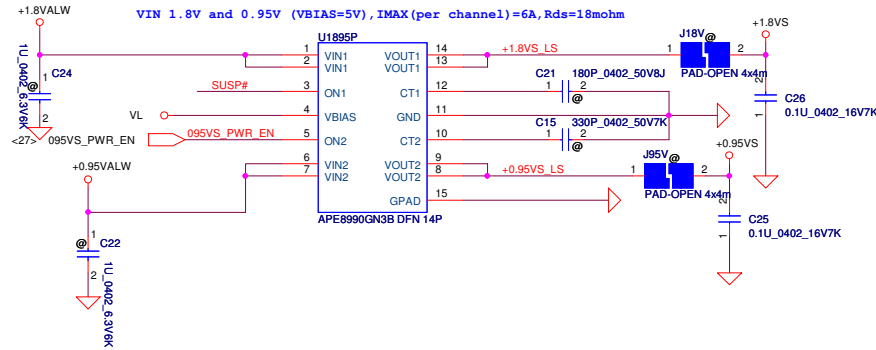




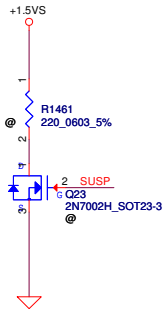
**+5VALW TO +5VS**  
**+3VALW TO +3VS**  
**Load switch**



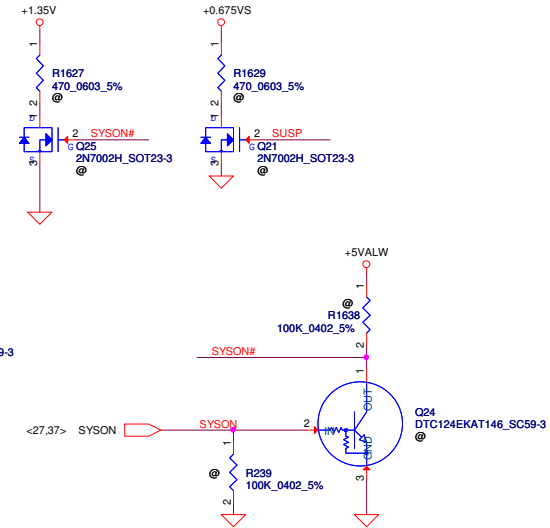
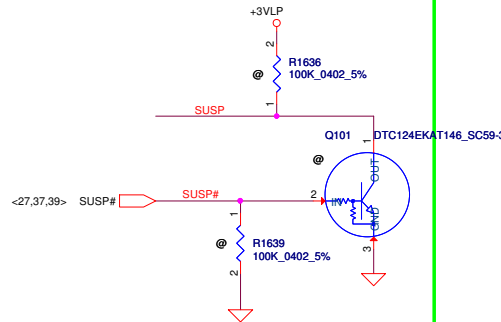
**+1.8VALW TO +1.8VS**  
**+0.95VALW TO +0.95VS**  
**Load switch**



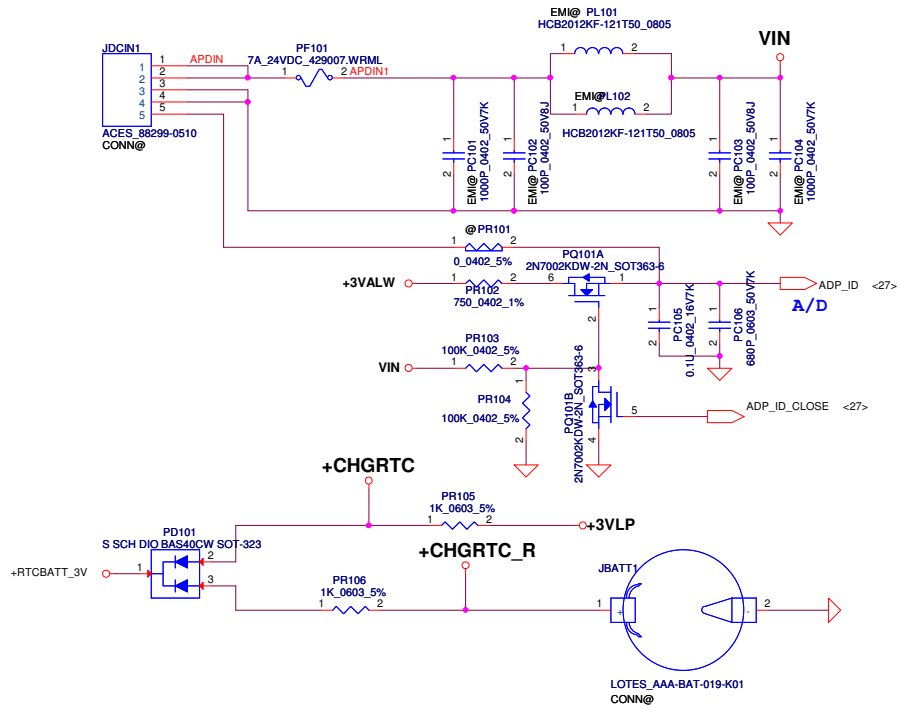
**+1.5VS discharge circuit only for Beema**  
**only 1.5VS from PWR**



**only for Beema**



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ADP_ID		
AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

RTC Battery

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Sheet 33 of 46					

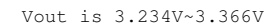




SY8208B\_V2.mdd

Change 3V5V\_EN to 3VALW\_EN

ENLDO\_3V5V



+5VALWP

SY8208C\_V2.mdd

5V LDO 150mA~300mA

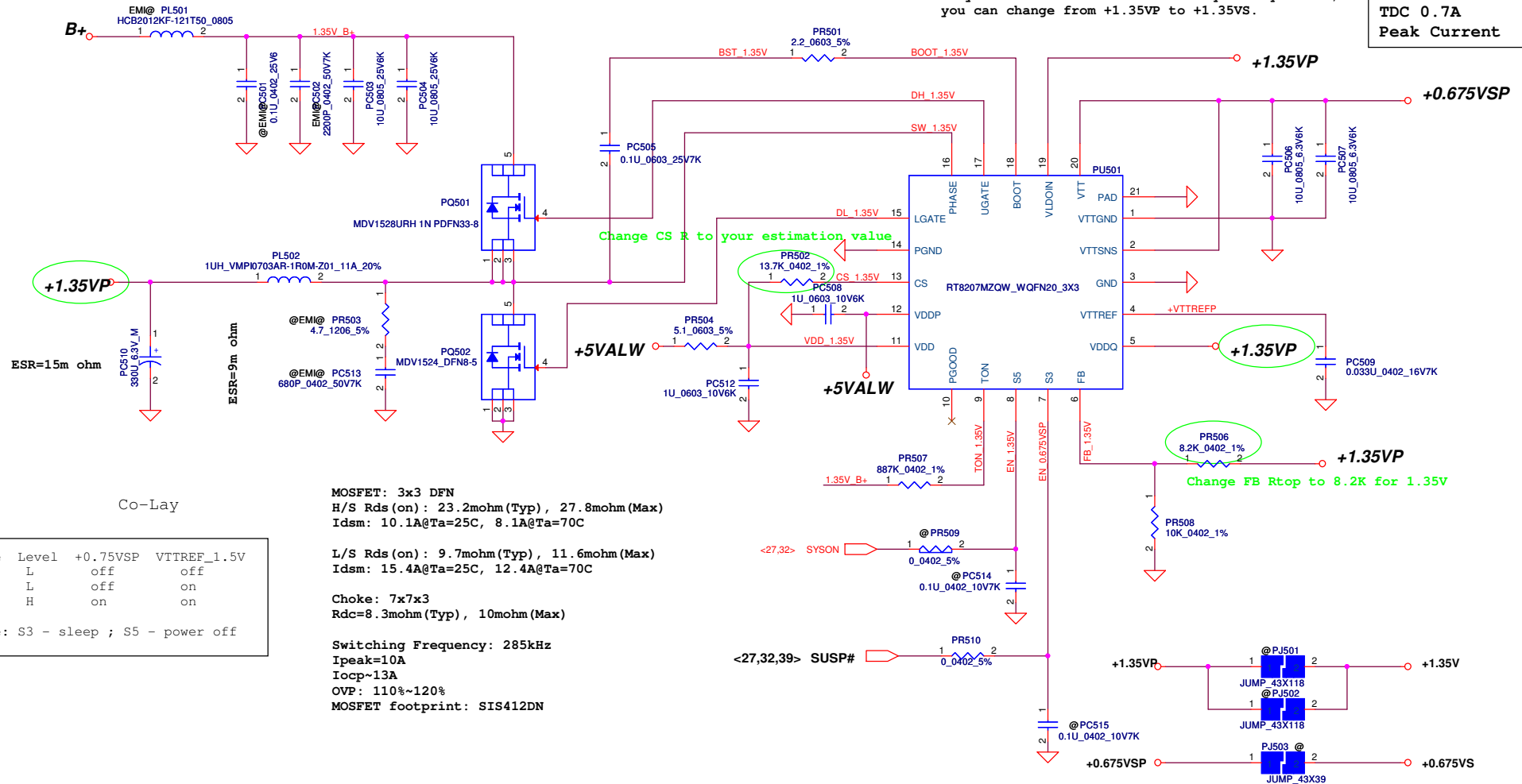
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Title	PWR- 3VALW/5VALW-SY8208B/C
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# Module model information

RT8207M\_V1.mdd For Single layer  
RT8207M\_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%  
TDC 0.7A  
Peak Current 1A

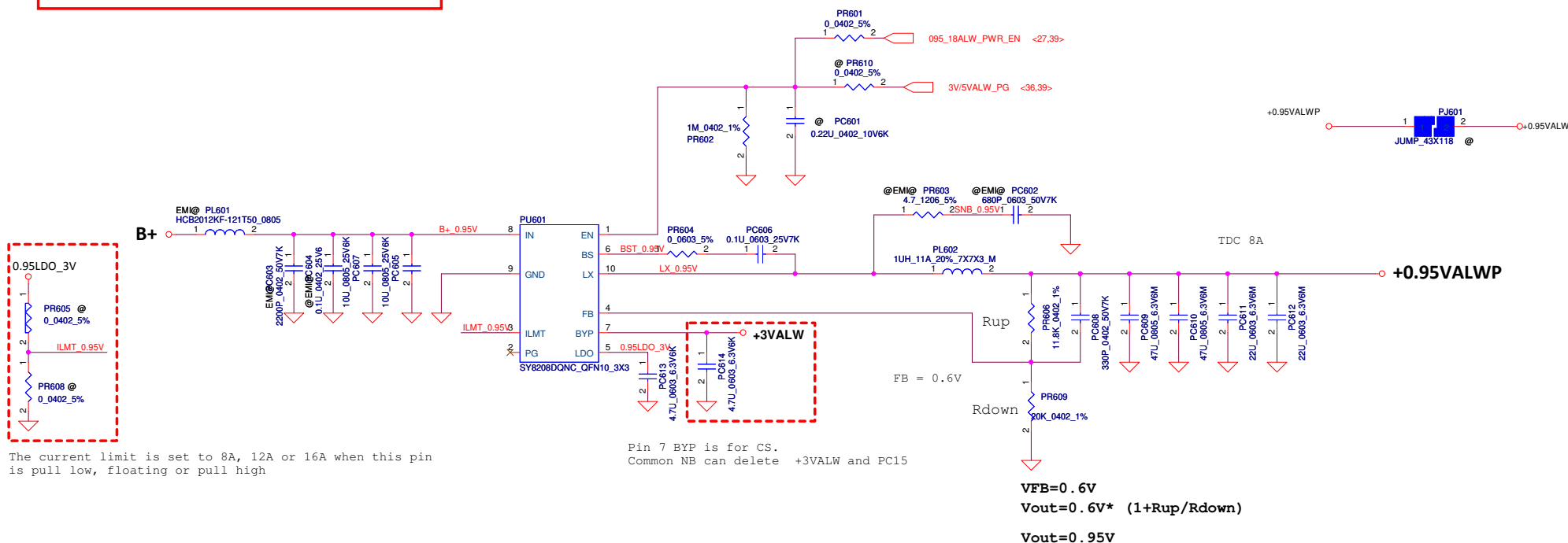


Security Classification		Compal Secret Data		Title	
Issued Date	2014/03/03	Deciphered Date	2015/03/03	Size	Document Number
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# Module model information

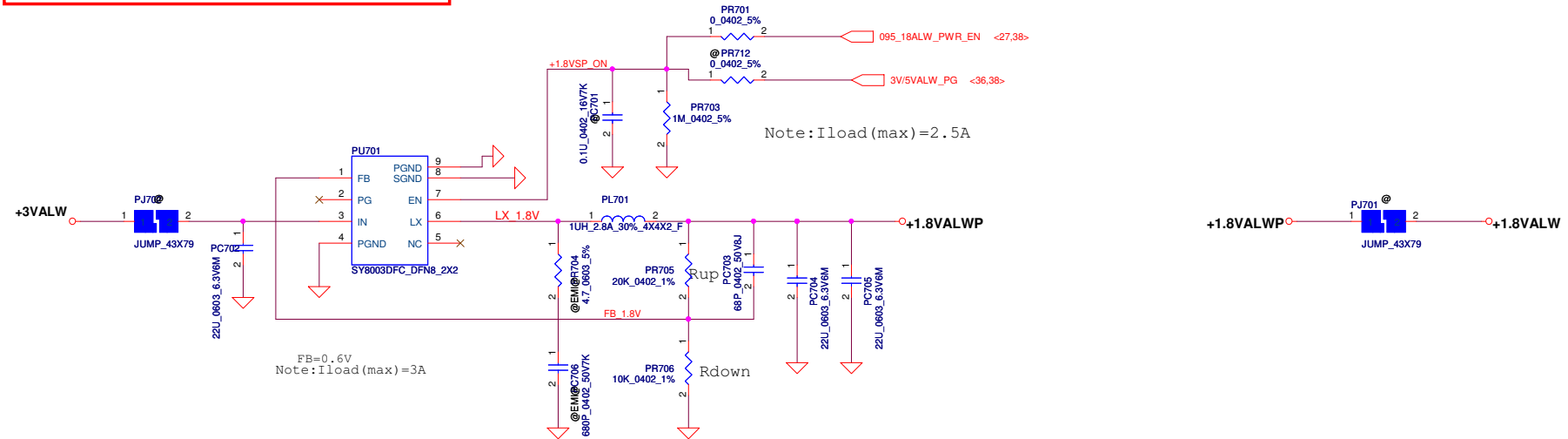
SY8208D\_V2.mdd

EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



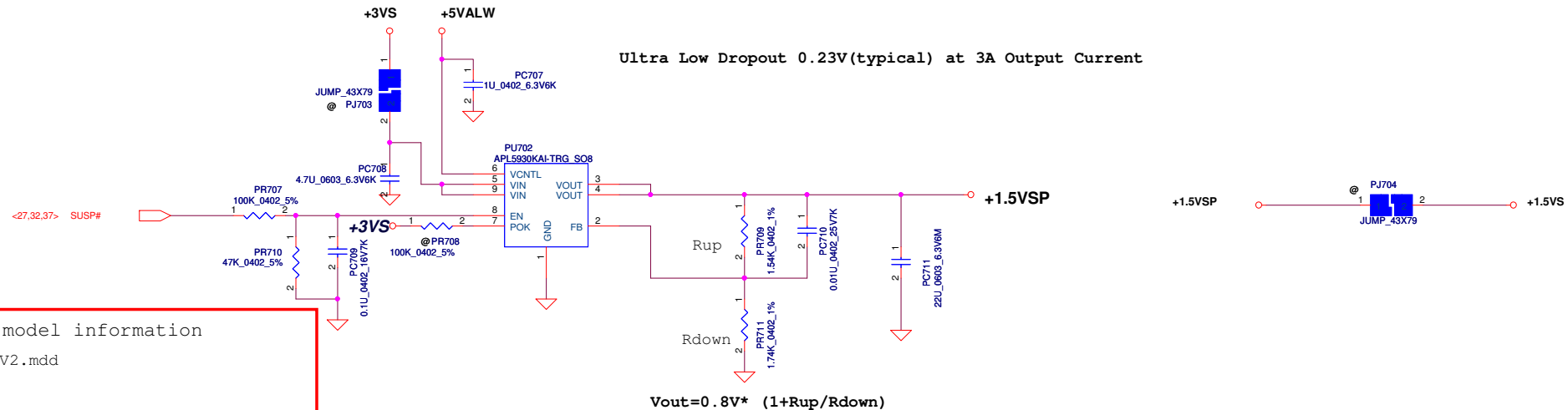
# Module model information

SY8003\_V2.mdd



Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

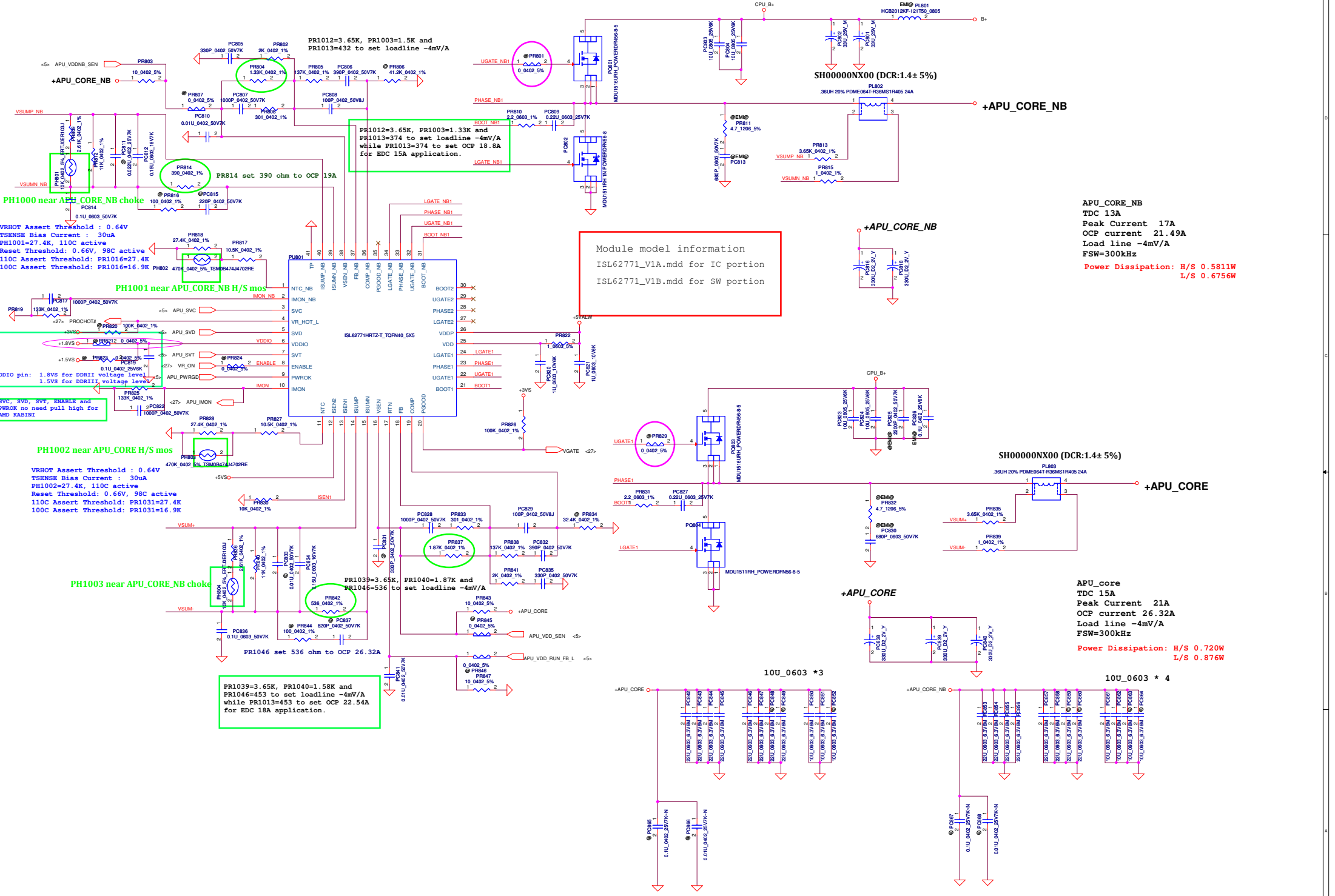
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$



# Module model information

APL5930\_V2.mdd

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APU\_CORE\_NB  
TDC 13A  
Peak Current 17A  
OCP current 21.49A  
Load line -4mV/A  
FSW=300kHz  
Power Dissipation: H/S 0.5811W  
L/S 0.6756W

APU\_core  
TDC 15A  
Peak Current 21A  
OCP current 26.32A  
Load line -4mV/A  
FSW=300kHz  
Power Dissipation: H/S 0.720W  
L/S 0.876W

Module model information  
ISL62771\_V1A.mdd for IC portion  
ISL62771\_V1B.mdd for SW portion

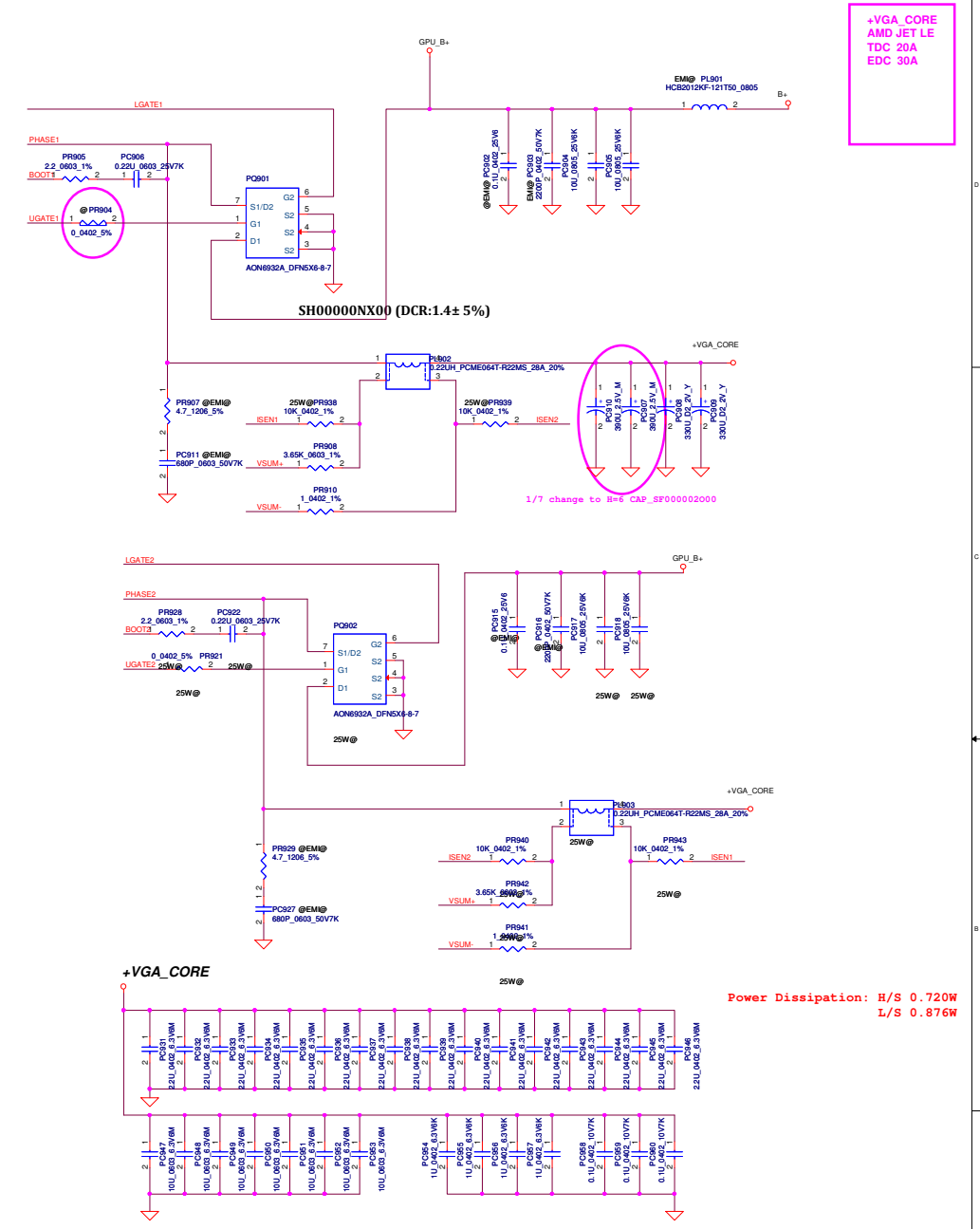
VRHOT Assert Threshold : 0.64V  
TSense Bias Current : 30uA  
PH1001=27.4K, 110C active  
Reset Threshold: 0.66V, 98C active  
110C Assert Threshold: PR1016=27.4K  
100C Assert Threshold: PR1016=16.9K

SVC, SVD, SVT, ENABLE and  
PWROK no need pull high for  
AMD KABINI

VRHOT Assert Threshold : 0.64V  
TSense Bias Current : 30uA  
PH1002=27.4K, 110C active  
Reset Threshold: 0.66V, 98C active  
110C Assert Threshold: PR1031=27.4K  
100C Assert Threshold: PR1031=16.9K

GPU 15W setting

PR931=536 ohm, PR924=1K ohm, PC925=0.1uF,  
PR944 = 0 ohm, PR920=10K ohm,  
PC961 @, PC962 @, PR938 @ and PR939 @  
while PR931=536 ohm to set OCP for GPU 15W application.



+VGA\_CORE  
AMD JET LE  
TDC 26A  
EDC 30A

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